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## Third Semester B.E. Degree Examination, June/July 2019 Digital Electronics

Time: 3 hrs.

Max. Marks: 80

**Note: Answer any FIVE full questions, choosing  
ONE full question from each module.**

### Module-1

- 1 a. Write the switching equation for a digital circuit with four inputs and whose output is '1' if majority of its inputs are '1'. (04 Marks)
- b. Place the following equations into proper canonical forms and write its decimal notations also :
- i)  $P = f(a, b, c) = a\bar{b} + a\bar{c} + bc$
- ii)  $Q = f(x, y, z) = (x + \bar{y})(\bar{y} + z)$ . (06 Marks)
- c. Solve using k – map and implement using only NAND gates  
 $B = f(w, x, y, z) = \Sigma(1, 2, 3, 4, 9) + \Sigma d(10, 11, 12, 13, 14, 15)$ . (06 Marks)

**OR**

- 2 a. Solve using K Map  
 $A = f(w, x, y, z) = \pi(1, 2, 3, 4, 8, 9, 10, 11, 12, 13, 14, 15)$   
 and implement using NOR gates only. (06 Marks)
- b. Simplify using Quine Mc Clusky method :  
 $D = f(a, b, c, d) = \Sigma(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$   
 Show the prime implicant table to determine the EPIs. (10 Marks)

### Module-2

- 3 a. Design a combinational circuit that multiplies two 2bit binary values, and produces 4-bit product. Get the minterms for  $P_0, P_1, P_2$  and  $P_3$ . Simplify only for  $P_2$ . (08 Marks)
- b. Design a 4 to 16 decoder using 3 to 8 decoders (74LS138) only and realize the function :
- $P = f(w, x, y, z) = \Sigma(1, 4, 8, 13)$
- $Q = f(w, x, y, z) = \Sigma(2, 7, 13, 14)$ . (08 Marks)

**OR**

- 4 a. Design a 2 bit magnitude comparator and get an expression for  $A < B$  only, which is the minimal expression. (08 Marks)
- b. Explain a carry look ahead adder with a neat diagram and relevant expressions. (08 Marks)

### Module-3

- 5 a. Explain an SR latch using NOR gates with circuit diagram function table and timing diagram. (06 Marks)
- b. Explain a positive edge triggered D flip flop with circuit diagram, function table and timing diagram. (10 Marks)

OR

- 6 a. What is race around? How is it overcome in master slave JK F/F. Explain MS JK with relevant circuit diagram, function table. (10 Marks)
- b. Derive the characteristics equation for : (06 Marks)
- i) SR F/F ii) JK F/F iii) D F/F iv) T F/F.

**Module-4**

- 7 a. Given an universal shift register, sketch its diagram only for left shift operates and explain its working. (08 Marks)
- b. What is a twisted ring counter? Sketch its diagram and explain its counting sequence and also give the bits that determine a state uniquely. (08 Marks)

OR

- 8 a. Design a model synchronous counter for the sequence, using a D flip-flop [Refer Fig.Q8(a)].

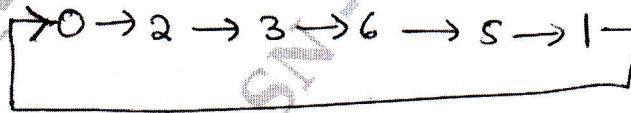


Fig.Q8(a)

- b. Explain with net diagram, the counting sequence and timing diagram, the working of a 4 bit binary ripple counter, using positive edge triggered T flip flop. (08 Marks)

**Module-5**

- 9 a. Draw and explain the Mealy and Moore sequential circuit models. (06 Marks)
- b. Analyze the following sequential circuit and draw its state diagram.[Refer Fig.Q9(b)]. (10 Marks)

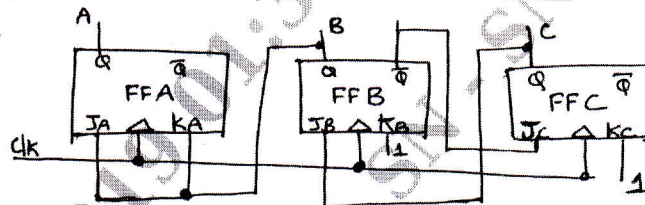


Fig.Q9(b)

OR

- 10 a. Represent a Moore circuit notation of a JK flip-flop through state diagram and explain. (06 Marks)
- b. Design a modulo 8 synchronous counter with : (10 Marks)
- i) state diagram ii) state table iii) transition table iv) excitation table, kmap and logic diagram

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